What is Claimed:

1. A chip carrier comprising:

a base,

an inner well formed about the periphery of the base; and

an outer well formed about the periphery of the inner well.

2. The chip carrier according to claim 1 wherein the first well and the second well form a flexible structure.

3. The chip carrier according to claim 1 wherein the outer well includes an outer wall and an inner wall and the inner well includes an outer wall coupled to the inner wall of the outer well.

4. The chip carrier according to claim 1 further comprising an upper surface and wherein the outer well extends farther away from the upper surface than the inner well.

5. The chip carrier according to claim 1 further comprising an integrated circuit positioned on the base.

6. The chip carrier according to claim 1 wherein the outer well and the inner well are continuous.

7. The chip carrier according to claim 1 wherein at least one of the outer well and the inner well are not continuos.

8. A process of manufacturing an integrated circuit comprising:

providing the integrated circuit;

providing a chip carrier including a base, an inner well formed about the periphery of the base, and an outer well formed about the periphery of the inner well; and

positioning the integrated circuit on the base.

9. The process of claim 8 further comprising sealing the integrated circuit in the chip carrier.

10. The process of claim 9 further comprising providing the chip carrier with a continuous outer well.

11. The process of claim 8 further comprising shipping the chip carrier from a first location to a second location.

12. A method for manufacturing an electronic component comprising:

receiving a chip carrier including a base, an inner well formed about the periphery of the base, an outer well formed about the periphery of the inner well, and an integrated circuit positioned on the base; and

retrieving the integrated circuit from chip carrier.

13. The method according to claim 12 further comprising positioning the retrieved integrated circuit on a circuit board.

14. A carrier comprising:

an upper surface defining a first reference plane;

a first wall extending away from the reference plane towards a first position;

a second wall extending away from the first position towards the reference plane;

a third wall extending away from the reference plane towards a second position; and

a base positioned below the first reference plane

15. The carrier according to claim 14 wherein the first position is further from the reference plane than the second position.

16. The carrier according to claim 14 wherein:

the base defines a second reference plane positioned below the first reference plane;

the third position is located below the second reference plane; and

the first position is located below the second reference plane.

17. The carrier according to claim 14 wherein the first wall and the second wall form a first well.

18. The carrier according to claim 17 wherein the third wall and the fourth wall form a second well.

19. The carrier according to claim 14 wherein the third wall and the fourth wall form a well.

20. A method of transporting a device comprising:

providing a carrier including a base, an inner well formed about the periphery of the base, and an outer well formed about the periphery of the inner well; and

moving the device from a first location to a second location in the carrier